PRODUCT SPECIFICATION

4108E-S

IEEE 802.11ah Wireless LAN

Module Datasheet

Version:v1.0

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

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4108E-S Module Datasheet

	Part NO.	Description
Ordering Information	FG4108ESXX-01	MM6108,802.11ah,1G,WIFI,1T1R,13X13,SDIO+SPI,with SAW

CONTENTS

Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2024/11/01	New version	Lxp	Lxy	Qjp

1. General Description

1.1 Introduction

4108E-S is an IEEE 802.11ah Wi-Fi module designed in compliance with the IEEE 802.11ah standard, supporting data rates up to 32.5 Mbps that operates in the Sub 1GHz license-exempt band, offering longer ranger and higher data rate for internet of things (IoT) applications. 4108E-S enables streamlined data transfer interoperability with existing Wi-Fi networks while meeting up to 1Km long range data transfer with low power consumption requirements.

4108E-S integrated IEEE 802.11ah Sub-1G 8MHz Single-chip MAC/PHY/Radio SoC Morse Micro MM6108, ultra-long-reach PA, high linearity LNA, T/R switch, 32 MHz crystal and it has been designed for a simplified Wi-Fi HaLow connection to an external host for applications in which a customer wants to merely replace their prior RF technology with a Wi-Fi HaLow connection while leveraging the latest WPA3 security protocol. supports SDIO 2.0 compliant slave interface and SPI mode operation, and many peripherals such as general I2C, UART and GPIOs. In addition, its MAC supports for STA and AP roles.

1.2 Description

Model Name	4108E-S
Product Description	IEEE 802.11ah Wireless LAN Module
Major Chipset	Morse Micro MM6108 (48-pin QFN)
Form Factor	LGA module, 44 pins
Dimension	L x W x H: 13 x 13 x 2.25mm
Host Interface	SDIO/SPI
Antenna	For Stamp Module, “1T1R, external” ANT Main：TX/RX
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 85°C

2. Features

General

- Support 850 - 950MHz frequency band
- Support single-stream data rate up to 32.5Mbps @8MHz or 15 Mbps @4MHz channel.
- Support channel width options of 1/2/4/8 MHz
- Support Modulation and Coding Scheme (MCS) levels MCS 0-7 and MCS 10
- Modulation: BPSK & QPSK, 16-QAM & 64 -QAM
- Support for 1 MHz and 2 MHz duplicate modes

Host Interface

- SDIO 2.0 (slave) Default Speed (DS) at 25MHz
- SDIO 2.0 (slave) High Speed (HS) at 50MHz
- Support for both 1-bit and 4-bit data mode
- Support for SPI mode operation

Standards Supported

- IEEE Std 802.11ah-2016 compliant

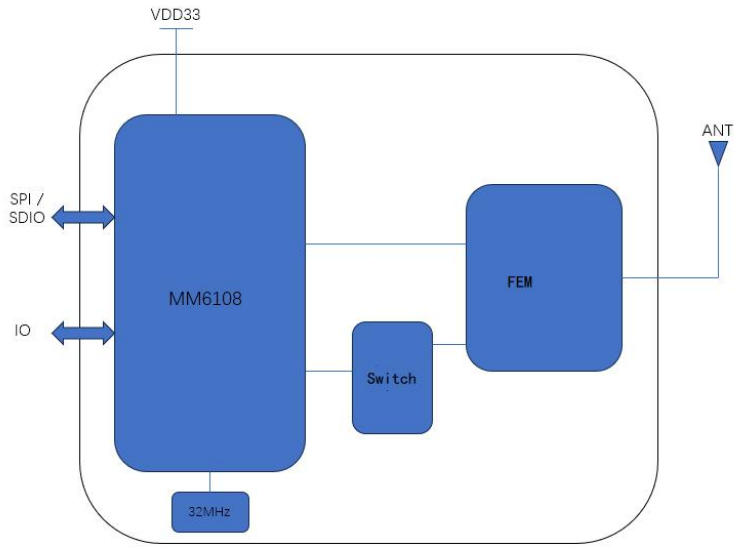
Security Features

- AES encryption engine
- Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
- WPA3 including protected management frames (PMF)
- Opportunistic Wireless Encryption (OWE)

Peripheral Interfaces

- SDIO/SPI, I2C and UART
- Support for STA and AP roles

3. Block Diagram



4. General Specification

4.1 WLAN Specification

Feature	**Description**	
WLAN Standard	IEEE 802.11ah	
Frequency Range	850 - 950 MHz	
Channel Bandwidth	1/2/4/8 MHz	
Modulation	OFDM, BPSK, QPSK, 16-QAM, 64-QAM	
Test Items	**Typical Value**	
Output Power	MCS0 (1/2/4/8 MHz) : 21dbm±2dB	
	MCS7 (1/2/4/8 MHz) : 16dbm±2dB	
	MCS10 (1 MHz) : 21dbm ±2dB	
Receive Sensitivity	- MCS0 (1 MHz)	-105
	- MCS0 (2 MHz)	-102
	- MCS0 (4 MHz)	-99
	- MCS0 (8 MHz)	-95
	- MCS7 (1 MHz)	-87
	- MCS7 (2 MHz)	-81
	- MCS7 (4 MHz)	-80
	- MCS7 (8 MHz)	-76

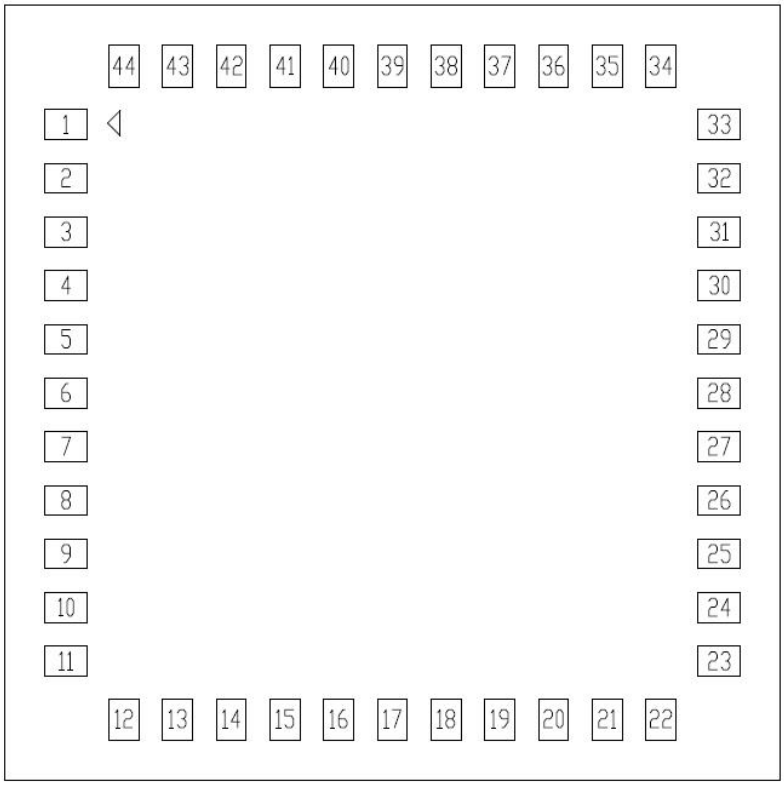
	- MCS10 (1 MHz)	-106
Data Rate	1 MHz Bandwidth: up to 3.333Mbps 2 MHz Bandwidth: up to 7.222Mbps 4 MHz Bandwidth: up to 15Mbps 8 MHz Bandwidth: up to 32.5Mbps	
Security	■ AES encryption engine ■ Hardware support for SHA1 and SHA2 hash functions (SHA-256,SHA-384,SHA-512) ■ WPA3 including protected management frames (PMF) ■ Opportunistic Wireless Encryption (OWE)	

* If you have any certification questions about output power please contact FAE directly.

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage

1	GND		Ground connections	
2	ANT	I/O	RF IN/OUT	
3	GND		Ground connections	
4	NC		No Connection	
5	NC		No Connection	
6	MM_WAKE	I	WAKE from sleep	
7	NC		No Connection	
8	NC		No Connection	
9	VBAT		3.3V power supply	3.3V
10	GND		Ground connections	
11	GND		Ground connections	
12	MM_RESET_N	I/O	Reset (active low)	
13	NC		No Connection	
14	MM_SD_D2	I/O	SDIO Data pin 2	
15	MM_SD_D3	I/O	SDIO Data pin 3	
16	MM_SD_CMD	I/O	SDIO Command pin	
17	MM_SD_CLK	I	SDIO Clock pin (input)	
18	MM_SD_D0	I/O	SDIO Data pin 0	
19	MM_SD_D1	I/O	SDIO Data pin 1	
20	GND		Ground connections	
21	NC		No Connection	
22	VDDIO		I/O supply Input	1.8V/3.3V
23	NC		No Connection	
24	NC		No Connection	
25	MM_GPIO6	I/O	General purpose I/O	VDDIO
26	MM_GPIO5	I/O	General purpose I/O	VDDIO
27	MM_GPIO4	I/O	General purpose I/O	VDDIO
28	MM_GPIO3	I/O	General purpose I/O	VDDIO
29	MM_GPIO2	I/O	General purpose I/O	VDDIO
30	MM_GPIO1	I/O	General purpose I/O	VDDIO
31	GND		Ground connections	
32	MM_GPIO7	I/O	General purpose I/O	VDDIO
33	GND		Ground connections	
34	MM_GPIO11	I/O	General purpose I/O	VDDIO
35	MM_GPIO10	I/O	General purpose I/O	VDDIO
36	GND		Ground connections	
37	MM_GPIO9	I/O	General purpose I/O	VDDIO

38	MM_GPIO8	I/O	General purpose I/O	VDDIO
39	MM_JTAG_TDO	O	JTAG data output	
40	MM_GPIO0	I/O	General purpose I/O	VDDIO
41	MM_JTAG_TMS	I	JTAG mode selection	
42	MM_JTAG_TDI	I	JTAG data input	
43	MM_JTAG_TRST	I	JTAG reset	
44	MM_JTAG_TCK	I	JTAG clock	

P:POWER I:INPUT O:OUTPUT

5.3 Pin multiple Definition

PIN	NAME	Default function	IO function 0	IO function1	Further function
25	MM_GPIO6	GPIO	UART1 Rx	None	
26	MM_GPIO5	GPIO	I2C SCL	None	
27	MM_GPIO4	GPIO	I2C SDA	None	
28	MM_GPIO3	GPIO	UART0 Tx	PWM1 bit 3	
29	MM_GPIO2	GPIO	UART0 Rx	PWM1 bit 2	
30	MM_GPIO1	GPIO	PWM1 bit 1	None	1wire EEPROM
32	MM_GPIO7	GPIO	UART1 Tx	None	
35	MM_GPIO10	GPIO	SPI0 D0	None	
37	MM_GPIO9	GPIO	SPI0 CS0	None	
38	MM_GPIO8	GPIO	SPI0 SCK	None	
39	MM_JTAG_TDO	JTAG data output			
40	MM_GPIO0	GPIO	PWM1 bit 0	SPI0 CS3	

6. Electrical Specifications

6.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	-40	25	85	deg.C

VBAT	3.0	3.3	3.6	V
VDDIO	1.8	3.3	3.6	V

6.2 Power Consumption

Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V VBAT (mA) AVG.
915.5	MCS0	1	Tx @ 21 dBm	215
		2		218
		4		220
		8		225
	MCS7	1	Tx @17 dBm	165
		2		168
		4		170
		8		170
	MCS10	1	Tx @ 21 dBm	235
Band (MHz)	**Modulation**	**BW (MHz)**	**DUT Condition**	**VBAT = 3.3V VBAT (mA) Avg.**
915.5	MCS0	1	Continuous Rx @ -105 dBm	31
		2	Continuous Rx @-103dBm	33
		4	Continuous Rx @ -101 dBm	41
		8	Continuous Rx @ -97 dBm	53
	MCS7	1	Continuous Rx @ -87 dBm	31
		2	Continuous Rx @ -84 dBm	35
		4	Continuous Rx @-81 -8dBm	45
		8	Continuous Rx @ -77 dBm	58
	MCS10	1	Continuous Rx @ -107 dBm	40

The power consumption is based on Fnlink test environment, these data for reference only.

6.3 Interface Circuit time series

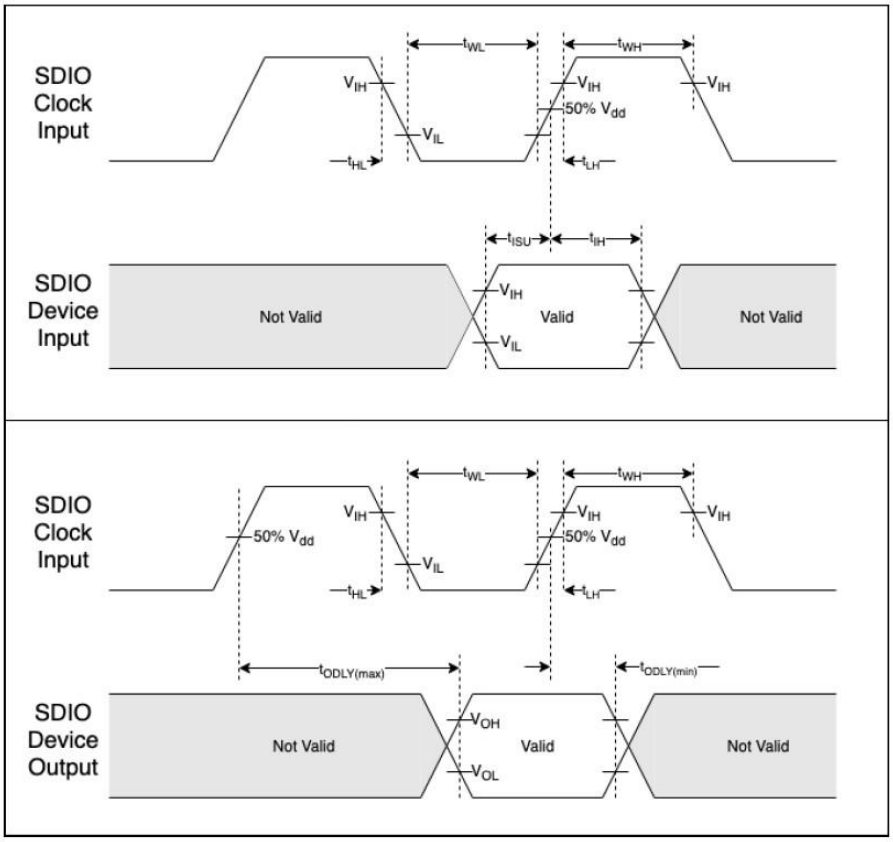
6.3.1 SDIO Bus Timing

PIN	NAME	SDIO4bit	SDIO1bit	SPI device mode	
14	MM_SD_D2	Data pin 2	Unused	Unused	

15	MM_SD_D3	Data pin 3	Unused	Chip select	
16	MM_SD_CMD	Command pin	Command pin	MOSI	
17	MM_SD_CLK	Clock (input)	Clock (input)	Clock (input)	
18	MM_SD_D0	Data pin 0	Data pin 0	MISO	
19	MM_SD_D1	Data pin 1	IRQ	IRQ	

Internally the SDIO will present two functions (in addition to the mandatory function 0) to be used to access the chip. Functions 1 and 2 only differ in the maximum transfer size they support. Function 1 can perform transactions up to 8 bytes at a time, function 2 supports up to 512 bytes at a time, making it better suited to bulk data transfers.

The SDIO clock rate supports up to 50MHz. The device always operates in SD high speed mode.



Parameter	Min	Max
Clock parameters		
Clock frequency	0MHz	50MHz
Clock low time (t_{WL})	7ns	
Clock high time(t_{WH})	7ns	
Clock rise time (t_{LH})		3ns
Clock fall time (t_{HL})		3ns
Inputs on CMD, DAT lines to device from host		
Input setup time (t_{ISU})	6ns	
Input hold time (t_{IH})	2ns	
Outputs on CMD, DAT lines from device to host		
Output delay ($t_{ODLY(max)}$)		14ns
Output hold time ($t_{ODLY(min)}$)	2.5ns	
Total system capacitance for each line		40pF

6.3.2 SPI Bus

The SPI interface uses the physical unidirectional pin layout as defined below, over which the modified SDIO protocol is used for communication.

PIN	NAME			SPI device mode	
14	MM_SD_D2			Unused	
15	MM_SD_D3			Chip select	
16	MM_SD_CMD			MOSI	
17	MM_SD_CLK			Clock (input)	
18	MM_SD_D0			MISO	
19	MM_SD_D1			IRQ	

After power-on, the host interface can be either SDIO or SPI. As per the SDIO specification,to switch the interface to SPI mode, the host must send a CMD0 while holding CS low (its asserted state).For further details on the protocol, see the SD Specification Part E1 “SDIO Simplified Specification” version 2.00.

The SPI clock rate supports up to 50MHz. The SPI bus timing is identical to the SDIO bus timing, where MOSI and MISO are considered input and output timing, respectively, in the SDIO timing specification.

The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per SDIO high-speed mode. It may be configured to behave like CPHA=0 (drive output

on negative edge, sample on positive edge) after being initialized.

6.3.3 UART Bus

Two universal asynchronous receiver/transmitter (UARTs) are available and provide a means for serial communication to off-chip devices. The UART cores are as-provided by the SiFive IP repository. The UART peripheral does not support hardware flow control or other modem control signals, or synchronous serial data transfers.

We will clock the UARTs with a maximum clock speed of 30MHz (TBD), meaning maximum baud of the UART will be around 30Mbaud or 30Mbits/s if a divisor of 0 is specified.

The UART peripheral supports the following features:

- 8-N-1 and 8-N-2 formats: 8 data bits, no parity bit, 1 start bit, 1 or 2 stop bits
- 8-entry transmit and receive FIFO buffers with programmable watermark interrupts
- 16× Rx oversampling with 2/3 majority voting per bit

Pin	Name	Default Function	I/O Function
32	MM_GPIO7	GPIO	UART1 Tx
25	MM_GPIO6	GPIO	UART1 Rx
28	MM_GPIO3	GPIO	UART0 Tx
29	MM_GPIO2	GPIO	UART0 Rx

6.3.4 I2C Bus Timing

An I2C master interface is available. It consists of two lines, SDA and SCL, which are bidirectional, connected to a positive supply voltage via a current-source or pull-up resistor.

Pin	Name	Default Function	I/O Function
27	MM_GPIO4	GPIO	I2C SDA
26	MM_GPIO5	GPIO	I2C SCL

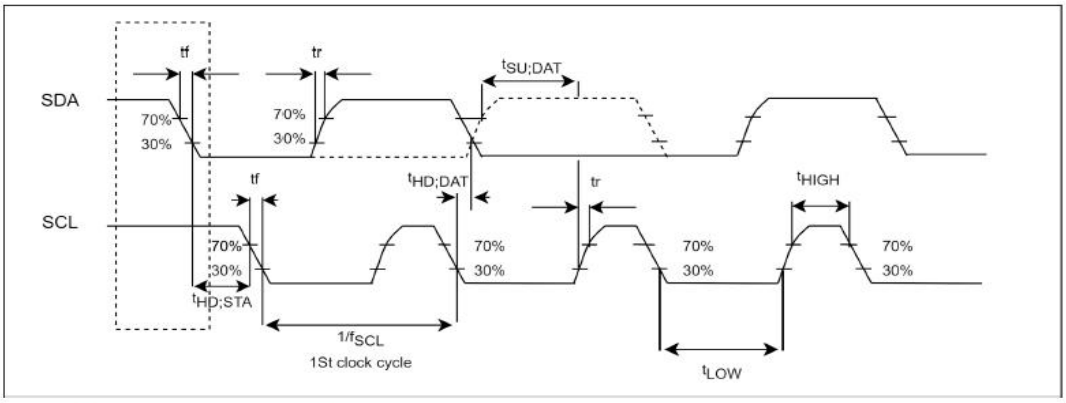
8-bit oriented, bidirectional data transfers can be made at

- Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s Serial
- High-speed mode (Hs-mode),with a bit rate up to 3.4M/bits

Data on the I

2C bus can be transferred at rates of up to 100kbit/s in Standard-mode, up to 400kbit/s in Fast-mode, up to 1 Mbit/s in Fast-mode Plus.

Definition of timing for F/S-mode devices on the I2C-bus. All values referred to



$V_{IH(min)}(0.3V_{DD})$ and $V_{IL(max)}(0.7V_{DD})$levels.

Parameter	Standard-mode		Fast-mode	
	Min	Max	Min	Max
Clock frequency(f_{SCL})	0	100kHz	0	400kHz
Fall time of both SDA and SCL (t_f)	-	300ns	20x (V_{DD}/5.5V)	300ns
Rise time of both SDA and SCL signals(t_r)	-	1000ns	20ns	300ns
Data hold time ($t_{HD;DAT}$)	5.0us	-	-	-
Data set-up time ($t_{SU;DAT}$)	250ns	-	100ns	-
LOW period of the SCL clock	4.7us	-	1.3us	-
HIGH period of the SCL clock	4.0us	-	0.6us	-
Hold time- START,first clock is generated after this($t_{HD;STA}$)	4us	-	0.6us	-

6.3.5 PWM

The pulse-width modulation (PWM) block can generate multiple types of waveform on GPIO pins via register settings, and can also be used to generate several forms of internal timer interrupt. There are two instances of PWM IP available. The PWM cores are as-provided by the SiFive IP repository.

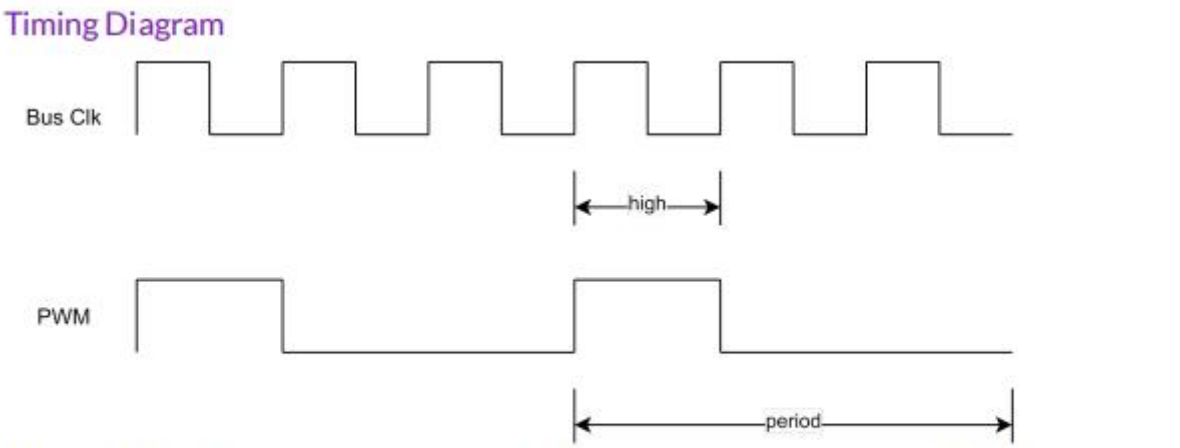
This IP operates on standard GPIO pins. See pin Description below for more details.

The PWM block is fully programmable. The output period and high time (duty cycle) can be modified at any

time by the target application through register programming.

- generation of multiple types of waveform on GPIO output pins
- used to generate several forms of internal timer interrupt
- comparator results are captured in flops and then fed to the PLIC as potential interrupt sources
- comparator outputs are further processed by an output ganging stage before being fed to the GPIOs
- IP can be provided in different comparator precisions up to 16 bits

Please refer to the SiFive spec - PWM section for more information.



'High and 'period' can be adjusted through the register programming and PWM waveforms vary depending on the ratio.

6.3.6 JTAG

A JTAG interface is provided for chip debug and test purposes. Its circuitry will not be reset by anything other than the reset from the JTAG interface pin. [Ensure pin 44 (JTAG_RST) is tied to the ground during chip boot.] This may cause problems when the chip is power-cycled whilst JTAG is not in reset.

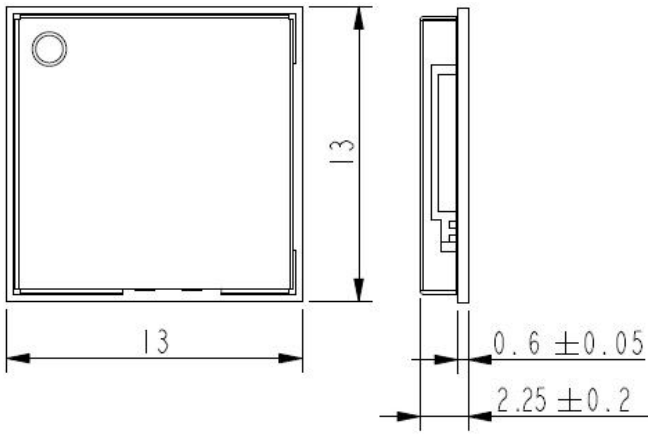
Functionally the JTAG will be the standards-compliant protocol interface and provide access to:

- custom internal test logic enables (scan mode, MBIST mode)
- SiFive RISC-V debug logic for CPU and system debug
- Morse custom JTAG overrides “Get-out-of-Jail” (GooJ) block registers

It will be constrained to 50MHz in mission/functional and scan modes.

7. Size reference

7.1 Module Picture

L x W : 13 x 13 (±0.2) mm 	
H: 2.25 (±0.2) mm	
Weight	0.7g

7.2 Marking Description

< TOP VIEW >

备注：

二维码内容：112233445566;FG4108ESXX-01

1.Fn-Link 商标 logo

2.机型：4108E-S

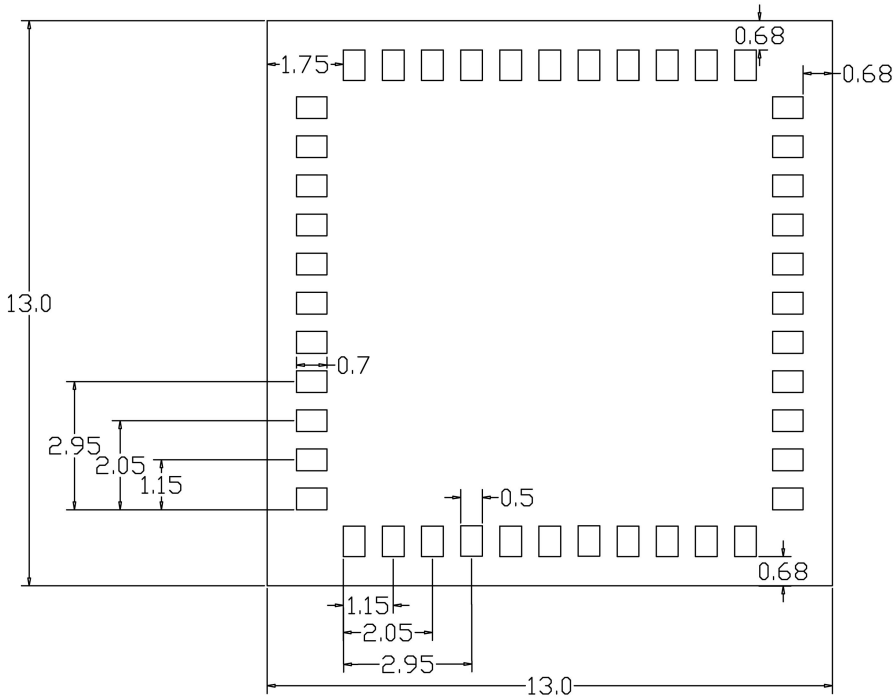
3. 二维码：编码规则为“mac 地址;成品料号”

例如：112233445566;FG4108ESXX-01（MAC 地址以实际为准）

4.V/N 01(V/N 到 01 之间为两个空格，01 为成品料号后缀，与二维码右对齐）

7.2 Physical Dimensions

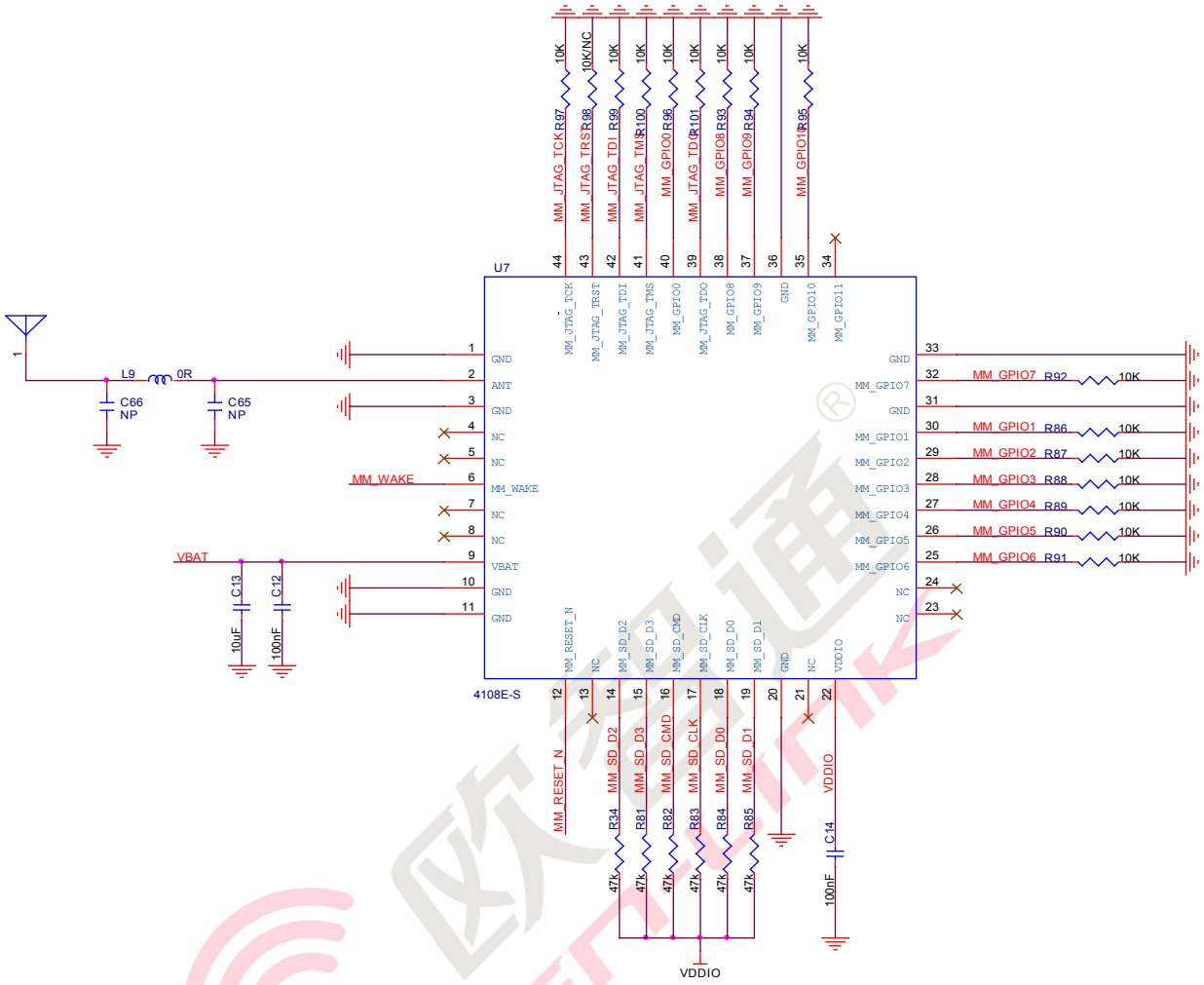
<TOP View>



8.The Key Material List

Item	Part Name	Description	Manufacturer
1	Crystal	2016 32MHZ,8PF,±10PPM,-30-85℃	ECEC,TKD,Hosonic ，JWT
2	Chipset	MM6108IQ-T,IEEE 802.11ah Sub-1 GHz 1/2/4/8MHz Bandwidth MAC/PHY/Radio SoC,QFN48	Morse Micro
3	PCB	4108E-S-V2.0 深绿色,6 层板, HDI,FR4,无卤 TG150,金厚 2μ",13X13X0.6mm	XY-PCB,GDKX, Sunlord, SLPCB
4	Shielding	4108E-S-V1.0 屏蔽盖,12.15*12.15*1.65mm,洋白铜,无定位脚,无绝缘层	信太，精力通,卓益
5	FEM	860 to 930MHz,2.0-4.8V,+27dbm,MCM 16pin,3.0 x 3.0 x 0.75 mm	Skyworks,KX
6	Switch	0.1-6.0GHz, 0.5dB insertion loss at 2GHz,QFN6	Richwave,GSR
7	Filter	B39921B2625P810,FILTER SAW 915MHZ 5SMD	Qualcomm/RF360

9. Reference Design

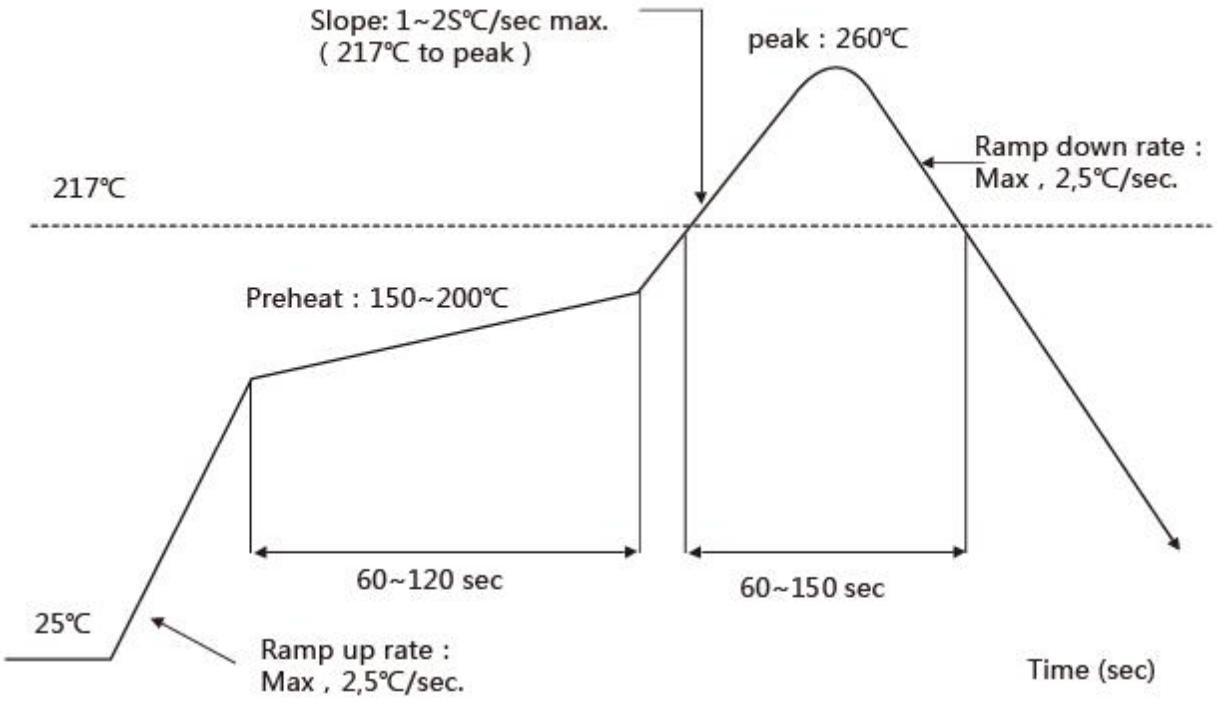


10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

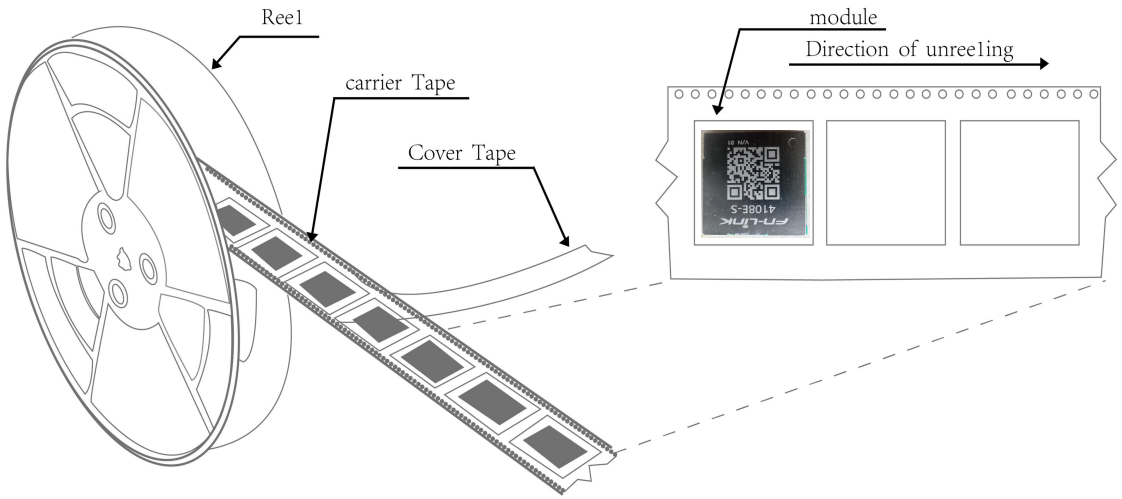
Number of Times : ≤2 times



11. Package

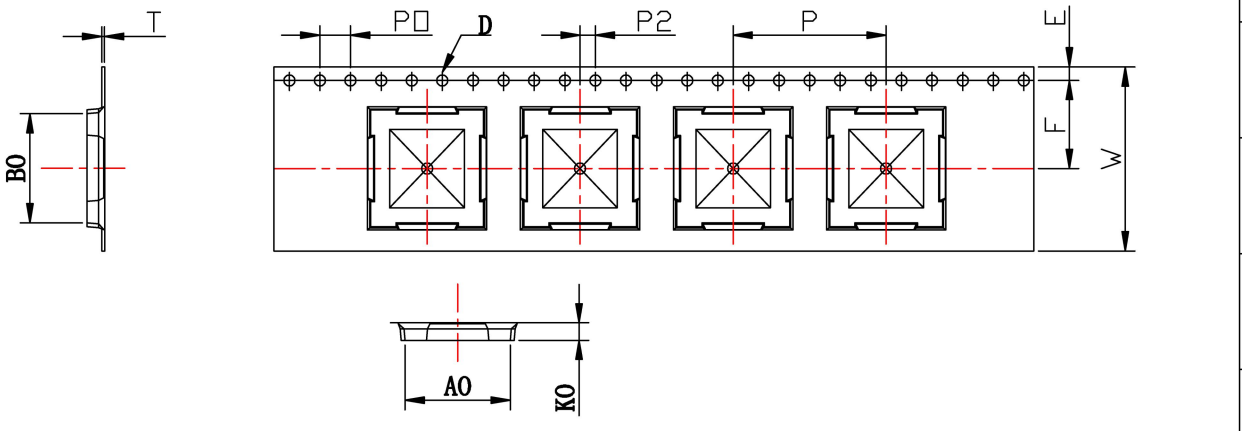
11.1 Reel

A roll of 1500pcs



11.2 Carrier Tape Detail

ITEM	W	AO	BO	D	F	E	KO	PO	P2	P	T
DIM	24	13.35	13.95	1.50	11.5	1.75	2.30	4.0	2.0	20.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	+0.1 -0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



11.3 Packaging Detail

the take-up package

Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape :21.3mm*32.6m

Color of plastic disc: blue

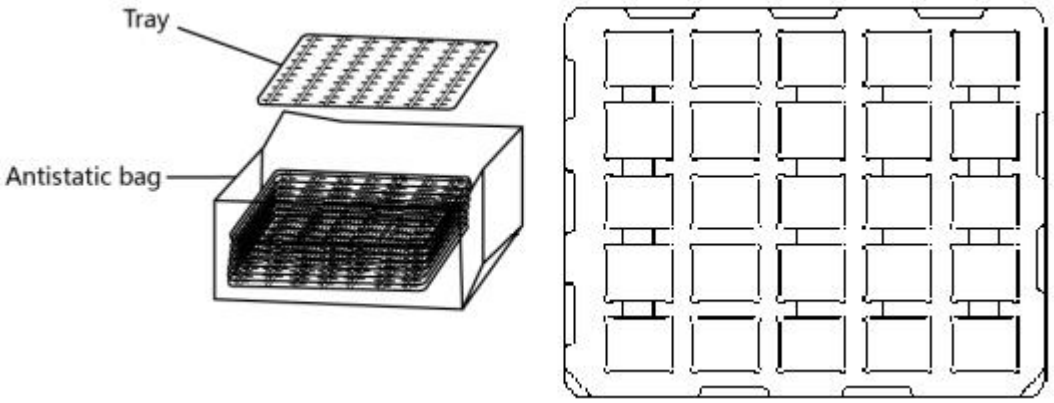
NY bag size:460mm*385mm

size ： 350*350*35mm

The packing case size:350*210*370mm

11.4 Tray

Use pallet packaging for less than 300 pieces



12. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more